UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/716,378	11/21/2000	Kazumasa Mine	OSP-9705	8330

21254 7590 10/02/2003

MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 10/02/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/716,378	MINE, KAZUMASA	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 21 November 2000 and 07 July 2003 .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 21 November 2000 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2, 5, 6 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-18 have been considered.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: IDS as received on 21 November 2000; Priority Papers as received on 21 November 2000; Change of Address as received on 21 November 2000; IDS as received on 20 March 2002; and IDS as received on 07 July 2003.

Drawings

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: Figure 12, element S290H. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claim 3 is objected to because of the following informalities: Please correct claim 3, line 3 which states "instruction set for which data present under the control of said main processor

needs to" with --instruction set for which data *presently* under the control of said main processor needs to--. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

8. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

9. Claims 1, 2, 8-10, 12-16, and 18 are rejected under 35 U.S.C. 102(e) as being taught by Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy).

10. Referring to claim 1, Levy has taught a microprocessor system for executing instructions described in a program comprising:

a. A main processor for executing by means of hardware those instructions which belong to a first instruction set (Levy Abstract; column 2, lines 49-63; Figure 2; and Figure 3) and for executing by means of software those instructions which

belong to a second instruction set (Levy Abstract; column 9, lines 46-59; column 10, lines 4-36; Figure 2; and Figure 3); and

b. A co-processor operative under the control of said main processor for autonomously fetching an instruction belonging to said second instruction set to execute same by means of its hardware (Levy Abstract; column 2, lines 35-63; column 8, lines 34-41; column 9, lines 42-46; Figure 2; and Figure 3).

11. Referring to claim 2, Levy has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set which said co-processor cannot process by itself and issues a notification of said encounter to said main processor to thereby request the main processor to execute said specific instruction (Levy Abstract; column 9, lines 46-59; column 10 ,lines 4-36; Figure 2; Figure 3; Figure 6; and Figure 7).

12. Referring to claim 8, Levy has taught wherein said co-processor further comprising:

a. A stack memory for holding data generated in the course of execution of an instruction which belongs to said second instruction set (Levy Abstract; column 7, lines 61-64; column 11, lines 1-14; and Figure 3);

b. A stack pointer for holding an address of the most recent data in said stack memory (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12); and

c. A hardware resource for carrying out a process for updating said stack pointer among processes which take place in the course of execution of said specific instruction (Levy column 12, lines 26-31 and Figures 8-12).

13. Referring to claim 9, Levy has taught wherein said co-processor comprising:

a. A program counter for holding an address of an instruction which is currently processed and belongs to said second instruction set (Levy column 5, lines 18-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7); and

b. A hardware resource for carrying out a process for updating said program counter among processes which take place in the course of execution of said specific instruction (Levy column 5, lines 18-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7).

14. Referring to claim 10, Levy has taught wherein said co-processor comprises a status register for holding information indicative of a need of said notification and wherein said main processor periodically accesses said status register to recognize, from content of said status register, that said co-processor has encountered said specific instruction to thereby execute said specific instruction (Levy column 5, lines 18-42; column 7, lines 29-64; column 8, lines 21-24; Figure 3; Figure 6; and Figure 7).

15. Referring to claim 12, Levy has taught wherein said co-processor further comprises an instruction queue for holding a fetched instruction which belongs to said second instruction set (Levy column 8, lines 34-41; column 9, lines 42-59; and Figure 3) and wherein said main processor refers to said instruction queue of said co-processor to specify an interrupt handler which corresponds to said specific instruction to be executed (Levy column 9, lines 42-59; Figure 6; and Figure 7).

16. Referring to claim 13, Levy has taught wherein said co-processor has a stack architecture (Levy Abstract; column 5, lines 31-59; and Figure 3).

17. Referring to claim 14, Levy has taught a stack memory provided outside said co-processor (Levy Abstract; column 7, lines 61-64; column 11, lines 1-14; and Figure 3), wherein said co-processor further comprises a stack-top register for holding a predetermined number of top data of stack data (Levy column 5, lines 18-42; column 7, lines 29-42; Figure 3; and Figures 8-12).

18. Referring to claim 15, Levy has taught wherein said co-processor further comprises a cache memory provided between said stack memory and said stacktop register for caching a part of data held in said stack memory (Levy column 11, lines 1-14; Figure 3; and Figure 10).

19. Referring to claim 16, Levy has taught wherein said co-processor detects a predetermined instruction for which stack data needs to be manipulated over said stack-top register and said stack memory (Levy column 12, lines 1-43 and Figures 8-12), whereupon said co-processor moves contents of said stack-top register to said stack memory (Levy column 12, lines 1-43 and Figures 8-12) and thereafter requests said main processor to execute said predetermined instruction (Levy column 6, lines 50 to column 7, line 24), said main processor referring to contents of said stack memory, to which said contents of said stack-top register have been moved (Levy column 12, lines 1-43 and Figures 8-12), to thereby execute said predetermined instruction (Levy column 12, lines 1-43 and Figures 8-12). In regards to Levy, the example embodiment completes stack instructions in the co-processor, but, as is stated in column 6, line 50 to column 7, line 24 of Levy, the co-processor may send these instructions to the host.

20. Referring to claim 18, Levy has taught a program memory in which instructions belonging to said second instruction set are contained, wherein said co-processor further comprises:

a. A program counter for holding an address of an instruction that is currently processed and belongs to said second instruction set (Levy column 5, lines 8-42; column 7, lines 29-42; column 9, lines 42-46; Figure 3; Figure 6; and Figure 7);

b. An instruction queue for holding instructions which belong to said second instruction set (Levy column 8, lines 34-41; column 9, lines 42-59; and Figure 3); and

c. An instruction fetch circuit for fetching an instruction belonging to said second instruction set from said program memory using a value contained in said program counter as its address and for setting the fetched instruction to said instruction queue (Levy column 5, lines 8-42; column 7, lines 29-42; column 8, liens 34-41; column 9, lines 42-59; Figure 3; Figure 6; and Figure 7).

Claim Rejections - 35 USC § 103

21. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

22. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy), as applied to claim 2 above, and in view of Irwin, U.S. Patent Number 4,695,945 (herein referred to as Irwin). Levy has not explicitly

taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set for which data present under the control of said main processor needs to be handled to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself. However, Levy has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself (Levy Abstract; column 9, lines 46-59; column 10 ,lines 4-36; Figure 2; Figure 3; Figure 6; and Figure 7). Irwin has taught wherein said co-processor detects an encounter with a specific one of the instructions belonging to said second instruction set for which data present under the control of said main processor needs to be handled to thereby determine that said co-processor has encountered a specific instruction which cannot be processed by itself (Irwin Abstract; column 2, lines 39-64). A person of ordinary skill in the art at the time the invention was made, and as stated in Irwin, would have recognized that detecting this type of encounter is necessary to identify possible problems of contention for system resources (Irwin column 2, lines 22-24). By identifying these encounters, the processors resolve the resource contention and allow for processing to continue. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the encounter detection of Irwin in the device of Levy to resolve resource contention.

23. Claims 4-7 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy), as applied to claim 2 above, and in view of Schmidt et al., U.S. Patent Number 5,727,227 (herein referred to as Schmidt).

24. Referring to claims 4-7 and 11, Levy has taught:

a. Wherein said co-processor issues said notification by means of dedicated interrupt assigned in advance respectively to a predetermined number of ones of the instructions belonging to said second instruction set which have a higher frequency of execution than the other instructions (Applicant's claims 4) (Levy Abstract; column 6, line 50 to column 7, line 24; Figure 6; and Figure 7)

b. Wherein said main processor further comprises an interrupt request reception circuit for encoding said dedicated interrupt vectors sent from said co-processor (Applicant's claim 11) (Levy column 8, lines 21-24; column 9, lines 46-59; column 10, lines 4-36; Figure 3; Figure 6; and Figure 7).

25. Levy has not taught:

a. Interrupt vectors (Applicant's claim 4)

b. Wherein each of said dedicated interrupt vectors is assigned to a plurality of instructions belonging to said second instruction set (Applicant's claim 5)

c. Wherein priorities are set to a plurality of ones of said dedicated interrupt vectors (Applicant's claim 6)

d. Wherein a single instruction is assigned to a given one of said dedicated interrupt vectors to which a higher priority is set, while a plurality of instructions are assigned to a given one of said dedicated interrupt vectors to which a lower priority is set (Applicant's claim 7)

e. Specify an interrupt handler which corresponds to said specific instruction to be processed (Applicant's claim 11).

26. Schmidt has taught:

a. Interrupt vectors (Applicant's claim 4) (Schmidt column 3, lines 4-42)

b. Wherein each of said dedicated interrupt vectors is assigned to a plurality of instructions belonging to said second instruction set (Applicant's claim 5) (Schmidt column 3, lines 4-42).

c. Wherein priorities are set to a plurality of ones of said dedicated interrupt vectors (Applicant's claim 6) (Schmidt column 3, lines 4-42). In regards to Schmidt, the priority is inherent since the current process in the host is interrupted in order for the exception to be completed before the host processor completes the operation it was operating before the interrupt.

d. Wherein a single instruction is assigned to a given one of said dedicated interrupt vectors to which a higher priority is set, while a plurality of instructions are assigned to a given one of said dedicated interrupt vectors to which a lower priority is set (Applicant's claim 7) (Schmidt column 3, lines 4-42). In regards to Schmidt, the table includes information on the interrupts which includes whether the handler routine is one instruction or a plurality of instructions.

e. Specify an interrupt handler which corresponds to said specific instruction to be processed (Applicant's claim 11) (Schmidt column 3, lines 4-42).

27. A person of ordinary skill in the art at the time the invention was made would have recognized that an interrupt vector identifies information, including the address of the interrupt service routine, needed in order to execute the interrupt service routine. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to

incorporate the interrupt vector of Schmidt in the device of Levy to provide the information needed to access the interrupt service routine.

28. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Levy, U.S. Patent Number 5,923,892 (herein referred to as Levy), as applied to claim 1 above, and in view of Yamanaka, U.S. Patent Number 4,774,625 (herein referred to as Yamanaka). Levy has not taught a plurality of coprocessors in correspondence with a plurality of processes described in a program. Yamanaka has taught a plurality of coprocessors in correspondence with a plurality of processes described in a program (Yamanaka column 1, line 21 to column 2, line 28; Figure 1; and Figure 2). A person of ordinary skill in the art at the time the invention was made would have recognized that the plurality of coprocessors would allow for more operations to be executed simultaneously, thereby increasing speed of the processor. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the plurality of coprocessors of Yamanaka in the device of Levy to increase processor speed.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Kober et al., U.S. Patent Number 4,219,873, has taught a host processor with multiple co-processors.

b. Garner et al., U.S. Patent Number 5,109,514, has taught co-processors and how the system handles exceptions.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

31. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

32. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

September 29, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100